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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application		
Inventor	:	VAN LAMMEREN
Application No.	:	10/525,804
Filed	:	02/25/2005
For	:	VERSION-PROGRAMMABLE CIRCUIT MODULE

APPEAL BRIEF

On Appeal from Group Art Unit 2617

Date: 09/24/2007

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Michael Ure
(Name)

9/24/07
(Signature and Date)

TABLE OF CONTENTS

TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-15 are pending, of which claims 1-7 and 10-13 stand finally rejected and form the subject matter of the present appeal. Claim 8, 9, 14 and 15 have been objected to.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a version-programmable circuit module that allows a single circuit module to be versioned to provide a range of performance levels.

Such versioning may be achieved by providing a one-time-programmable (OTP) memory and programming the memory with a version number. An OTP memory, however, may require a different fabrication process than a circuit whose performance is to be versioned, thereby entailing costly modifications. To address this problem in a cost-effective way, the invention provides for a module having first and second sub-circuits, the first sub-circuit being the circuit whose performance is to be versioned. The first sub-circuit includes a version number memory. However, this memory need not be an OTP memory but rather can be a memory fabricated using the same process as the functional circuitry of the first sub-circuit. A second sub-circuit is provided having a write-protected memory (such as an OTP memory). The first and second sub-circuits are coupled by a communication link. A version number control circuit sends update values for the version number memory from the write-protected memory via the communication link. The invention is not intended to provide upgradeability.

In other embodiments, the version number memory is updated from the write-protected memory by multiplexing the version number with normal operating signals, for example placing the version number within the vertical blanking interval of a video signal.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A circuit module comprising	Figure 1	
a first and second sub-circuit and	Figure 1: 12, 14	Page 4, lines 4-8
a communication link coupled between the first and the second sub-circuit, the sub-circuits being	Figure 1, 16	Page 4, lines 9-14

arranged to communicate signals via the communication link during operation;		
the sub-circuit providing a performance dependent on the version number that is stored in the version number memory;	Figure 1, 14	Page 4, lines 15-23
the second sub-circuit comprising a write-protected memory and a version number control circuit arranged to send update values for the version number memory from the write-protected memory via the communication connection.	Figure 1: 120, 122, 124, 126	Page 4, line 24 to page 5, line 27

The following analysis of independent claim 10 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
10. A processor integrated circuit comprising:	Figure 1	
a write-protected memory;	Figure 1, 122	Page 4, lines 4-8
operating circuits arranged to provide a performance dependent on a version number that is stored in the write-protected memory;	Figure 1, 142	Page 4, lines 9-23
an external bus input;	Figure 1, 18	Page 3, line 24, to page 4, line 3
a communication bus output;	Figure 1, 16	Page 3, line 24, to page 4, line 3
a watchdog circuit coupled between the external bus input and the communication bus output,	Figure 1, 124	Page 4, line 24 to page 5, line 27
the watchdog circuit being arranged to pass commands from the external bus input to the communication bus output conditionally,	Figure 1, 124	Page 4, line 24 to page 5, line 27
the watchdog circuit detecting whether an update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write-protected memory.	Figure 1, 124	Page 4, line 24 to page 5, line 27

The following analysis of independent claim 11 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
11. A signal processing circuit comprising:	Figure 2	
a version number memory for storing a version	Figure 2, 242	Page 6, lines 28-32

number;		
operating circuits arranged to provide a signal processing with a performance dependent on a version number that is stored in the write-protected memory;	Figure 2, 142	Page 6, line 33 to page 7, line 11
an input and/or output for receiving and/or transmitting input signal to be processed or results of signal processing by said operating circuits;	Figure 2, 20	Page 6, lines 14-22; page 7, lines 12-16
a control circuit arranged to detect multiplexed data in a predetermined format of the input signal or result and to cause data from the input and/or output that is received during said time slot to be copied to the version memory.	Figure 2: 262, 260	Page 6, lines 28 to page 7, line 11

The following analysis of independent claim 12 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
12. A method of controlling operation of a circuit module, the method comprising		
providing a performance level of a first sub-circuit dependent on the version number that is stored in a version number memory;	Figure 2: 142, 140	Page 6, line 33 to page 7, line 11
passing a version number from a write-protected memory from a second sub-circuit of the circuit module to the version memory multiplexed with normal operating signals for the	Figure 2: 242, 24, 246	Page 6, line 33 to page 7, line 11

first sub-circuit.		

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102(a), claims 1-7 are anticipated by Easter.
2. under 35 USC 102(a), claim 10 is anticipated by Easter.
3. under 35 USC 102(a), claims 11 is anticipated by Easter.
4. under 35 USC 102(a), claims 12 and 13 are anticipated by Easter.

The rejection under 35 USC 112, second paragraph is not appealed.

VII. ARGUMENT

I. Rejection of Claims 1-7 as Anticipated by Easter

Easter relates to a system for providing secure upgradeability. As illustrated in Figure 6, signed configuration data is provided (from a disk 200, for example) to an upgradeable module 204 that includes a cryptographic configuration processor 210 and various functional chips 218, 220, etc. As described at column 7, lines 6-20, in operation, a secret key Ks is used to decipher a configuration signature that includes a new hardware configuration value Nc. Then the new hardware configuration value Nc is XORed with the result to obtain Ks(C), which is then deciphered using a public key Kp to obtain a configuration constant C. The configuration constant C thus obtained is compared with the configuration constant C stored in the cryptographic configuration processor. Only if they are the same is the new configuration Nc is loaded into the configuration register 214.

The rejection identifies the configuration register 214 of Easter as the first sub-circuit and the register 216 as the second sub-circuit.

The error in this rejection is that "update values for the version number memory" are not sent "from the write-protected memory via the communication connection." In Easter, the configuration register is updated or not updated depending on operations that use the contents of the register 216. Clearly, however, *update values* for the configuration register 214 are not *sent from* the register 216 via a communication connection.

Therefore Easter fails to anticipate the invention of claim 1.

With regard to dependent claims 2-7, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference.

Accordingly, these claims are also patently distinguishable and allowable over the cited reference by virtue of their dependency upon an allowable base claim.

II. Rejection of Claim 10 as Anticipated by Easter

Claim 10 is similar in many of its features to claim 1. Claim 10 claims in part a "watchdog circuit detecting whether an update command to update the version number is received and if so to pass said update command, *replacing a version number in the update command by a version number from the write-protected memory*."

As noted with respect to claim 1 above, in Easter, the configuration register is updated or not updated depending on operations that use the contents of the register 216. Clearly, however, a new configuration Nc in the update command is not *replaced by* information from the register 216.

Therefore Easter fails to anticipate the invention of claim 1.

III. Rejection of Claim 11 as Anticipated by Easter

In the invention of claim 11, once again the version number is stored in a write-protected memory and is copied to a version memory, again a feature that is absent from Easter.

Moreover, claim 11 specifies in greater detail the arrangement whereby the version number stored in the write-protected memory is communicated to the version memory, namely by multiplexing this information together with input data to the signal processing operating circuits. Easter also fails to teach or suggest this latter feature.

Therefore Easter fails to anticipate the invention of claim 11.

IV. Rejection of Claim 12 as Anticipated by Easter

Claim 12 relates to the arrangement whereby the version number stored in the write-protected memory is communicated to the version memory, namely by multiplexing this information together with normal operating signals for the sub-circuit. Considering the register 216 as the write-protected memory, in Easter, as previously established, this information is not communicated to the version memory at all, let alone in the manner recited.

Claim 13 further recites in part *replacing* a version number in an update command by a version number from the write-protected memory. As discussed previously in relation to claim 11, Easter contains no such teaching.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 9/24/07

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A circuit module comprising a first and second sub-circuit and a communication link coupled between the first and the second sub-circuit, the sub-circuits being arranged to communicate signals via the communication link during operation; the sub-circuit comprising a version number memory for storing a version number, the sub-circuit providing a performance dependent on the version number that is stored in the version number memory; the second sub-circuit comprising a write-protected memory and a version number control circuit arranged to send update values for the version number memory from the write-protected memory via the communication connection.

2. A circuit module according to claim 1 wherein the circuit module is a multi-component module, comprising a package that contains the first sub-circuit in a first integrated circuit and the second sub-circuit in a second integrated circuit.

3. A circuit module according to claim 1 wherein the control circuit is arranged to send the update values multiplexed with normal operating signals that are communicated between the first and the second sub-circuit.

4. A circuit module according to claim 3 wherein the communication connection is a communication bus coupled to the sub-circuits, the first sub-circuit being arranged to support execution of commands received via the communication bus, including an update command for updating the version number in the version number memory; the circuit

module comprising: an external bus input; the version number control circuit being a watchdog circuit coupled between the external bus input and the communication bus, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus conditionally, the watchdog circuit detecting whether the update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write protected memory.

5. A circuit module according to claim 4, comprising a processor integrated circuit containing a CPU and the write-protected memory, the first sub-circuit being a signal processing unit distinct from the processor integrated circuit, the CPU being arranged to provide a performance dependent on the version number that is stored in the write-protected memory.

6. A circuit module according to claim 5, wherein the watchdog circuit comprises a register, the circuit module being arranged to write a copy of the version number from the write-protected memory in the register on power up, the watchdog circuit replacing the version number in the command by the version number from the register.

7. A circuit module according to claim 2, wherein the first sub-circuit is a signal processing circuit having an input and/or output for receiving and/or transmitting input signals to be processed or results of signal processing, the performance determining a processing capacity for processing said signals and/or producing said results, the input

and/or output comprising the communication link over which the version number is communicated multiplexed with said input signals and/or results.

10. A processor integrated circuit comprising: a write-protected memory; operating circuits arranged to provide a performance dependent on a version number that is stored in the write-protected memory; an external bus input; a communication bus output; a watchdog circuit coupled between the external bus input and the communication bus output, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus output conditionally, the watchdog circuit detecting whether an update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write-protected memory.

11. A signal processing circuit comprising: a version number memory for storing a version number; operating circuits arranged to provide a signal processing with a performance dependent on a version number that is stored in the write-protected memory; an input and/or output for receiving and/or transmitting input signal to be processed or results of signal processing by said operating circuits; a control circuit arranged to detect multiplexed data in a predetermined format of the input signal or result and to cause data from the input and/or output that is received during said time slot to be copied to the version memory.

12. A method of controlling operation of a circuit module, the method comprising

providing a performance level of a first sub-circuit dependent on the version number that is stored in a version number memory; passing a version number from a write-protected memory from a second sub-circuit of the circuit module to the version memory multiplexed with normal operating signals for the first sub-circuit.

13. A method of controlling operation of a circuit module according to claim 12, the method comprising: receiving commands for the circuit module and distributing the commands to the first sub-circuit via a communication bus; monitoring received commands for an update command that commands updating of the version number in the version number memory and if so to pass said update command to the communication bus, replacing a version number in the update command by a version number from the write-protected memory.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE